

Amendments to the Claims:

The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

- 1        1. (currently amended) A method for optimizing the timing performance of  
2        an overall logic circuit where that overall logic circuit is implemented in a Field  
3        Programmable Gate Array (FPGA) with programmable interconnect of the  
4        FPGA behaving in a way such that the timing of logic signals routed by the  
5        programmable interconnect from a specific source to a specific load within the  
6        FPGA is affected negligibly by fanout to other logic loads connected to the same  
7        source signal, the method comprising the steps of:  
8            a) synthesizing the overall logic for first implementation in an FPGA, the  
9            synthesis including construction and first placement of the logic  
10           functions on the FPGA,  
11           b) analyzing the timing of the first implementation with the first placement,  
12           c) determining the most critical timing paths from analysis of the first  
13           implementation,

d) selecting as an object for improvement a specific critical path from the most critical timing paths,

e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signals contributing to that chosen critical path, such change being a change in the selection of logic elements and the placement of those elements which implement the critical path.

2. (currently amended) The method of Claim 1 in which the implementation of the critical logic in a new way in step e) is limited only to changes in the arrangement of the logic elements in the chosen critical path.

3. (currently amended) A method for optimizing the timing performance of overall logic circuit where that overall logic circuit is implemented in an GA with programmable interconnect of the FPGA behaving in a way such that the timing of logic signals routed by the programmable interconnect from a specific source to a specific load within the FPGA is affected negligibly by

6 fanout to other logic loads connected to the same source signal, the method  
7 comprising the steps of:  
8 a) synthesizing the overall logic for a base implementation in an FPGA, the  
9 synthesis including construction and placement of the logic functions on  
10 the FPGA,  
11 b) analyzing the timing of the base implementation,  
12 c) determining the most critical timing paths from analysis of the base  
13 implementation,  
14 d) selecting as an object for improvement a chosen critical path from the  
15 most critical timing paths,  
16 e) implementing in another way the critical logic in the chosen critical path  
17 with implementation of the critical logic performed with relative  
18 disregard as to the fanout of signals to other logic in the overall logic  
19 circuit and with placement of logic in the chosen critical path designed  
20 primarily to minimize the interconnected routing distance of the signals  
21 contributing to that chosen critical path, such change being a change in  
22 the selection of logic elements and the placement of those elements  
23 which implement the critical path.

24 f) modifying the placement of other logic in the overall logic circuit to  
25 accommodate the changes in placement of the chosen critical path while  
26 maintaining approximately the new placement of the critical logic,  
27 g) repeating steps b) through f) where the last implementation and placement  
28 of the overall logic circuit from step f) becomes the basis for starting  
29 again with this last implementation becoming the base implementation.

1 4. (currently amended) The method of Claim 3 in which the implementation  
2 of the critical logic in a new way in step e) is limited only to changes in the  
3 placement of the logic elements in the chosen critical path.